R E M A R K S

The present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

TELEPHONE INTERVIEW SUMMARY

In a telephone interview on December 11, 2007 between Examiner Desir and Applicant's representative, Robert Miller, the pending claims and the cited references were discussed. No agreement was reached.

COMPLETENESS OF OFFICE ACTION

The Office Action fails to address arguments presented by the Applicant in the previous response,[1] which are still relevant to the Demos reference being applied, as required by MPEP §707.07(f) and, therefore, is not complete as to all matters as required under 37 CFR §1.104. Specifically, MPEP §707.07(f) states that where Applicant's arguments are moot, the Examiner may use form paragraph 7.38. However, in an Examiner Note for form paragraph 7.38, MPEP §707.07(f) further states that "the examiner MUST, however, address any arguments presented by the applicant

[1] See page 2, line 20 through page 11, line 8 of the Amendment filed July 30, 2007.

which are still relevant to any references being applied" (MPEP §707.07(f), emphasis added by Applicant's representative).

The present Office Action states that "Applicant's arguments have been fully considered but are moot in view of the new ground of rejection necessitated by the amendment" (see page 5, section 3 of the Office Action). However, the new ground of rejection applies the Demos reference in the same manner as the Demos reference was applied in the previous Office Action[2]. In the Amendment filed July 30, 2007, Applicant presented arguments why the Demos reference did not disclose a scaler circuit as alleged by the Office. Since Demos is being applied in the present Office Action in the same manner as Demos was applied in the previous Office Action, the arguments present by the Applicant in the previous response are still relevant and, therefore, the Office must address those arguments. Since the current Office Action does not address the arguments presented in the previous response, as required by MPEP §707.07(f), the Office Action is not complete as to all matters as required under 37 CFR §1.104. As such, Applicant's representative respectfully requests the Office address the arguments presented in the previous response in a new Office Action or withdraw the rejection.

[2] Mailed May 7, 2007.

SUPPORT FOR CLAIM AMENDMENT

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 7 and 8, and in the specification as originally filed, for example, on page 11, line 3 through page 12, line 5, on page 13, lines 3-13 and on page 19, lines 9-19. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1-25 under 35 U.S.C. §103(a) as being unpatentable over Demos (U.S. Patent No. 5,988,863) in view of Soundararajan (U.S. Patent No. 7,039,113) has been obviated by amendment and should be withdrawn.

In contrast to Demos and Soundararajan, the presently claimed invention (claim 1) provides an apparatus comprising (a) a decoder circuit configured to receive an encoded video signal at a first input and to present a decoded video signal at a first output and (b) a scaler circuit configured (a) to receive the decoded video signal at a second input and a user input signal at a third input and (b) to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal are generated simultaneously by scaling the decoded video signal in

response to the user input signal. Claims 13 and 14 include similar limitations. Demos and Soundararajan do not appear to teach or suggest each and every element of the presently claimed invention, as required by MPEP §2143. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Specifically Demos does not teach or suggest a scaler circuit configured (a) to receive the decoded video signal at a second input and a user input signal at a third input and (b) to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal are generated simultaneously by scaling the decoded video signal in response to the user input signal, as presently claimed. In particular, FIG. 10 of Demos (cited by the Office on page 2 of the Office Action as corresponding to the apparatus of presently pending claim 1) shows four decoders 100, 102, 104 and 106 (see column 15, line 37 through column 16, ,line 11 of Demos). Decoders 100 and 102 each decode part (i.e., decoder 100 decodes only I- and P-frames, and decoder 102 decodes only B-frames) of a single encoded signal (i.e., Base Layer MPEG-2). Decoders 104 and 106 similarly decode a separate encoded signal (i.e., Enhancement Layer MPEG-2). The resolution of the output signals of the decoders 100, 102, 104 and 106 is

determined by the resolution of the respective encoded data streams (see column 15, lines 36-65 of Demos), not through scaling as presently claimed.

A person of ordinary skill in the art would not view a scaler circuit configured to present (i) a first video output signal having a first resolution at a second output and (ii) a second video output signal having a second resolution at a third output, where the first video output signal and the second video output signal **are generated simultaneously by scaling the decoded video signal** in response to the user input signal, as presently claimed, to be the same as using four decoders to generate four video signals, where each video signal has the same resolution as the encoded stream from which it is generated as disclosed by Demos. Therefore, Demos and Soundararajan do not appear to teach or suggest each and every element of the presently claimed invention, as required by MPEP §2143. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, one of ordinary skill in the art would not consider decoder circuits and scaler circuits to be interchangeable. In particular, substitution of a scaler circuit for the decoders 102, 104 and 106 of Demos would make the circuit in FIG. 10 of Demos unsatisfactory for its intended purpose and, therefore, there is nor suggestion or motivation for such

modification (see MPEP §2143.01). Soundararajan does not cure the deficiency of Demos. Therefore, Demos and Soundararajan do not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-12 and 15-25 depend, directly or indirectly, from either claim 1 or claim 14 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejections should be withdrawn.

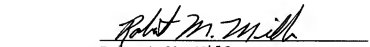
Accordingly, the present application is in condition for allowance. Early and favorable action by he Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative between 9:00 a.m. and 5:00 p.m. ET at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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Dated: December 17, 2007

c/o Lloyd Sadler
LSI Corporation

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